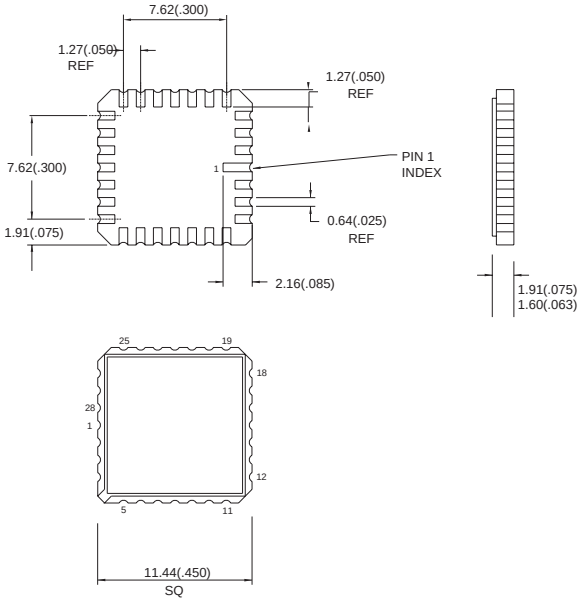
IRFQ110

MECHANICAL DATA
Dimensions in mm (inches)



LCC28 Ceramic Package

Pin 1 - Gate 1	Pin 2 - Source 1	Pin 3 - Source 1
Pin 4 - N/C	Pin 5 - Drain 1	Pin 6 - Drain 1
Pin 7 - N/C	Pin 8 - Gate 2	Pin 9 - Source 2
Pin 10 - Source 2	Pin 11 - N/C	Pin 12 - Drain 2
Pin 13 - Drain 2	Pin 14 - N/C	Pin 15 - Gate 3
Pin 16 - Source 3	Pin 17 - Source 3	Pin 18 - N/C
Pin 19 - Drain 3	Pin 20 - Drain 3	Pin 21 - N/C
Pin 22 - Gate 4	Pin 23 - Source 4	Pin 24 - Source 4
Pin 25 - N/C	Pin 26 - Drain 4	Pin 27 - Drain 4
	Pin 28 - N/C	

QUAD N–CHANNEL ENHANCEMENT MOSFETS

FEATURES

- **HERMETIC CERAMIC SURFACE MOUNT PACKAGE**
- **LIGHTWEIGHT**
- **MILITARY SCREENING LEVEL OPTIONS**
- **SPACE QUALITY LEVELS OPTIONS**

APPLICATIONS

- **FAST SWITCHING**
- **MOTOR CONTROLS**
- **POWER SUPPLIES**

ABSOLUTE MAXIMUM RATINGS FOR EACH CHIP (T_{case} = 25°C unless otherwise stated)

V_{DS}	Drain Source Voltage	100V
I_D	Continuous Drain Current	1A
I_D @T_C = 100°C	Continuous Drain Current	0.6A
I_{DM}	Pulsed Drain Current *	4A
V_{GS}	Gate Source Voltage	±20V
P_D	Maximum Power Dissipation	4.5W
$R_{\theta JC}$	Thermal Resistance Junction to Case	27.78°C/W
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +150°C

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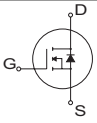
ELECTRICAL CHARACTERISTICS FOR EACH CHIP (T_{case} = 25°C unless otherwise stated)

	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
BV_{DSS}	Drain – Source Breakdown Voltage	V_{GS} = 0	I_D = 1mA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}	I_D = 250µA	2.0		4.0	
I_{GSSF}	Gate – Source Leakage Forward	V_{GS} = 20V				100	nA
I_{GSSR}	Gate – Source Leakage Reverse	V_{GS} = -20V				-100	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V.	V_{GS} =0			25	µA
			T_C = 125°C			250	
$R_{DS(on)}$	Static Drain Source On-State Resistance*	V_{GS} = 10V	I_D = 0.6A			0.70	Ω
		V_{GS} = 10V	I_D = 1.0A			0.80	
gfs	Forward Transductance *	V_{DS} = 15V	I_{DS} = 0.6A	0.86			S (℧)
C_{iss}	Input Capacitance	V_{GS} = 0	V_{DS} = 25V		180		pF
C_{oss}	Output Capacitance	f = 1MHz			82		
C_{rss}	Reverse Transfer Capacitance				15		
Q_g	Total Gate Charge	V_{GS} = 10V	V_{DS} = 50V			15	nC
Q_{gs}	Gate – Source Charge	I_{DS} = 1.0A				7.5	
Q_{gd}	Gate – Drain Charge					7.5	
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 50V	I_D = 1.0A			20	ns
t_r	Rise Time	R_G = 24Ω				25	
$t_{d(off)}$	Turn–Off Delay Time	(MOSFET switching times are essentially				40	
t_f	Fall Time	independent of operating temperature.)				40	
	BODY– DRAIN DIODE RATINGS & CHARACTERISTICS						
I_S	Continuous Source Current Body Diode	Modified MOS POWER symbol showing the intergal P-N junction rectifier. 				1.0	A
I_{SM}	Source Current* (Body Diode)					4.0	
V_{SD}	Diode Forward Voltage *	I_S = 1.0A	V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_F =1.0A	T_J = 25°C			200	ns
Q_{RR}	Reverse Recovery Charge	d_i / d_t = 100A/µs	V_{DD} = 50V			0.83	µC

Notes

* Pulse Test: Pulse Width ≤ 300µs, δ ≤ 2%

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